A Feasibility Demonstration Experimental Facility Simulation Of A Pasc Consolidation Inversion System For Faraday Connected MHD Generators

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A Feasibility Demonstration Experimental Facility Simulation of a PASC Consolidation/Inversion System For Faraday Connected MHD Generators

by

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ABSTRACT

A consolidation and inversion (CI), scheme based upon a Pulse-Amplitude-Synthesis-and-Control, (PASC), method of converter technology has been previously proposed for MHD generators. This paper describes the design, construction and initial test results obtained from a PASC Feasibility Demonstration Experimental Facility, (FDEF) constructed by the Electrical Engineering Department at Montana State University as part of the Feasibility Assessment Program for Space-Based, Multi-Megawatt Power Systems of the MHD/SDI office. Although the PASC converter technology can be applied to either Faraday or diagonally connected MHD generators, the FDEF has been configured initially to simulate approximately the conversion technology as it would be applied to Faraday type MHD generators because of the potential of the PASC technique for local, individual electrode control of the power extraction process and the resultant versatility of waveform synthesis which is desired for some SDI requirements.

After a brief introductory discussion of the PASC waveform synthesis procedure, the FDEF design is presented including: a) discussions on the real-time computer generated waveform synthesis algorithm used for triangular, square-wave, and sinusoidal waveforms, b) the design of the computer-switching matrix interface, c) design and implementation of the power injection gating and snubbing circuitry, d) the measurement system and data acquisition design.

Feasibility demonstration test results obtained using the FDEF are then discussed, including results for variable frequency sinusoids, triangular, and sawtooth waveforms as a function of dc source impedance and load impedance. Validation computer simulation results obtained using SPICE and EMTP generally agree closely with the experimental waveforms presented.

Finally, early computer simulation results for PASC CI of diagonal connected MHD generators are briefly discussed.

INTRODUCTION

The general problem MHD generator current equilization, consolidation and takeoff has received significant attention[1,2,3,4]. Because of the concentration on diagonal designs, consolidation work has been directed to some spreading of the total generator current out over the end electrodes of the diagonal generator along with the introduction of analog current ballancing circuits to force electrode current equilization for operation at off-design loading.

This paper describes a MHD/SDI funded Feasibility Demonstration Experimental Facility designed and constructed by the Electrical Engineering Department at Montana State University for the general study of dc power takeoff consolidation and waveform generation. The FDEF may be used to study consolidation and inversion of MHD Faraday or diagonal connected generators as well as arrays of other dc energy sources.

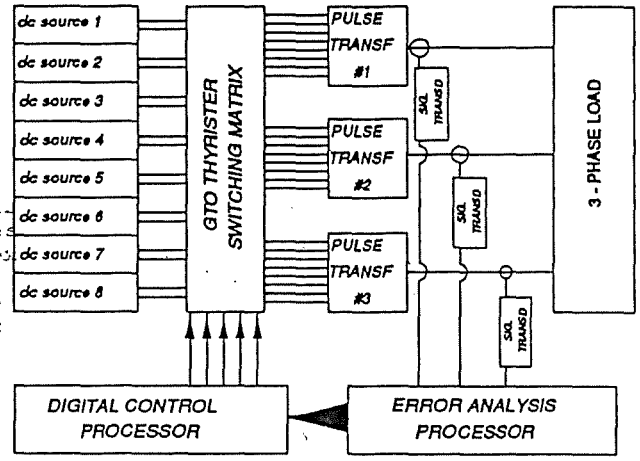

Figure 1 PASC FARADAY CONNECTED CI SYSTEM FOR EIGHT SOURCES

The basic synthesis technology utilized is called Pulse Amplitude Synthesis and Control (PASC) and has been briefly described in a 24th SEAM paper[3].

A functional block diagram of the PASC Faraday connection CI system is shown in Figure 1. The present FDEF implements all of the subsystem blocks shown in Figure 1 except that only open loop operation of the FDEF is presently implemented. A design for a very simple harmonic suppression controller is presently being studied by computer simulation. For purposes of illustration, eight sources are shown in Figure 1 which might represent eight independent or coupled sources of dc which are to be combined and inverted into commercial three phase power. There is no fundamental requirement for the sources to be all equal in characteristics although it is assumed that any source time dependence is of very low frequency in comparison with the frequency of output desired. For bipolar superposition of pulses such is required for commercial sinusoidal inversion, four of these sources would be used to generate positive pulses and four to generate negative pulses. For MHD Faraday type generator, pulse polarity reversal is simply obtainable by primary winding sense reversal on the consolidating pulse transformers.

The presently constructed FDEF consists of a set of 16 independently controllable d.c. power supplies whose outputs are connected by means of digitally switched Gate-Turnoff-Thyristors, (GTO's) to a system of pulse transformers which are used to directly synthesize pulsed approximations of a single-phase sinusoidal output to a load bank.

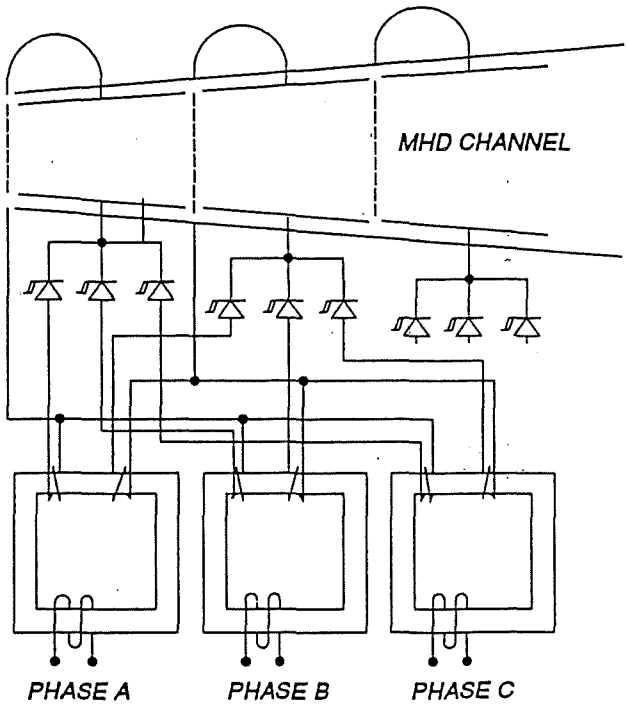

Figure 2 ADJACENT ELECTRODE PARALLEL LOADING TO OBTAIN BIPOLAR CONSOLIDATION AND 3 - PHASE INVERSION

A more complete commercially applicable system would consist of three such CI systems connected in parallel across the individual electrode outputs of a Faraday MHD generator as is illustrated in Figure 2. Such a loading scheme would guarantee that no electrode is ever open-circuited since in a three phase system there is always some current flowing in at least one of the phases. The figure illustrates one method used to obtain bipolar pulses from adjacent monopolarity MHD Faraday electrode pairs by winding reversal along with the parallel extraction of three phase power pulses. Although consolidation of every Faraday electrode pair is indicated, the necessity for reducing the complexity and gating expense will probably require consolidation of groups of several series connected electrode pairs resulting in a micro diagonal MHD configuration.

THE PASC WAVEFORM SYNTHESIS PROCEDURE

The basic PASC synthesis procedure involves extraction of energy from a set of dc sources in the form of nearly rectangular pulses, in a time overlapped manner, so as to digitally approximate the desired waveform. Assuming, to first order, that the sources are not time dependent and do not interact non-linearly, the consolidation is achieved in the present FDEF by means of ampere-turn flux additions in the primaries of a set of transformers which may be configured in either step-down or step-up, input-to-output voltage ratio as required to satisfy the desired load impedance. Although it was originally thought that exotic pulse transformer designs would be required for this process, FDEF experience indicates that regular commercial grade distribution transformers will suffice provided that the desired output waveform is three phase 60 Hz power. If the above assumptions on supply time invariance and/or supply non-uniformity of output are not met, the desired output may still be achievable (with some dynamic error), provided robust adaptive feedback control is applied. For some simple source failures, it is possible to redistribute the energy input deficit over the non-failing sources, provided the sources are reasonably similar in capability. For a fixed total number of sources, this will imply some additional harmonic distortion as well as reduction in total output energy delivered to the load.

a. Waveform Synthesis Algorithms

The load waveform synthesis algorithms presently implemented in the FDEF have been aimed at the generation of waveforms with zero dc content, because of the use of transformers as the basic consoidation and pulse forming elements. The digital synthesis algorithm for low harmonic ac waveforms was originally studied by Anderson, et al of NASA[5], who derived minimum harmonic waveform synthesis formulas for a given number of superposition pulses, in which there is complete control of pulse amplitude as well as duration. Although this algorithm could be implemented directly in the present FDEF by the use of non-uniform primary-to-secondary winding

turns ratios, the adjustment of the turns ratio would imply non-uniform electrode loading for a MHD generator which is not a desirable constraint. The alternative solution adopted in the present PASC FDEF implementation is to increase the number of fixed amplitude superposition pulses so as to achieve comparable harmonic purity.

As a simple waveform example of the synthesis procedure consider the algorithm for generating a linear slope triangular wave whose digital approximation is shown in Figure 3.

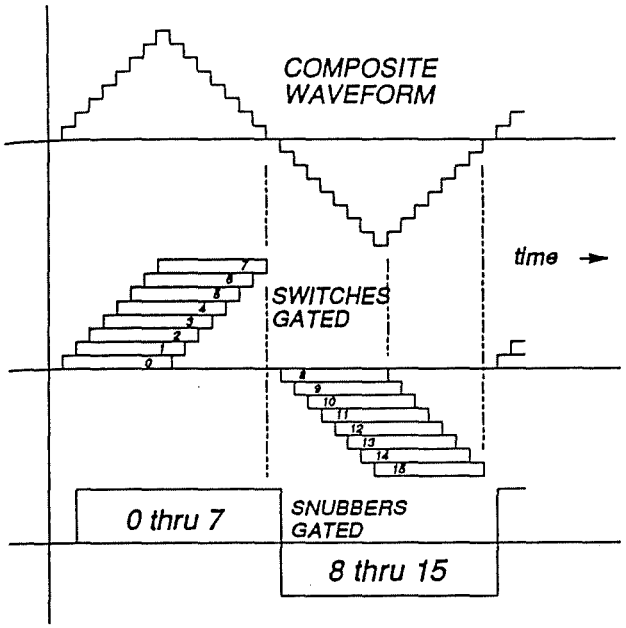

Figure 3 Triangular Waveform Synthesis Algorithm

Here the triangular waveform is generated by the time overlapped superposition of eight positive voltage pulses of equal duration followed by an identical sequence superposition of negative voltage pulses. Note the requirement for the voltage of the turned off successive positive pulses to be zero starting approximately at one quarter of a cycle through the waveform; this zero requirement is really zero (not open circuited), which is achieved by the inductive voltage spike controlling GTO's, or snubbers. Thus the snubbing GTO's are absolutely necessary for correct waveform generation while also limiting the magnitude of the induced voltage spikes (and dissipation), to very low levels. For sinusoidal voltage generation, the switching times are sinusoidal rather than constant but the pulse widths are still very nearly equal. Near rectangular square wave pulses can be achieved by simply gating on all of the positive sources simultaineously for the desired positive pulse duration followed by simultaineous positive snubbing before repeating the algorithm for the negative pulse sources to achieve the negative portion of the cycle. Although non-uniform pulse widths may be necessary to synthesize a desired waveform, the power duty cycle of each electrode source group can be averaged to the same value simply by permuting the pulse width duty cycle over successive cycles. This is very easy to achieve in the control program.

b. Computer Switching Matrix Interface

The switching control algorithms used in the PASC process are all digital in nature and reside in a single-master/multi-slave controller, which consists of a master minicomputer (Digital Microvax II), with input/output bus mounted slave switch commutation controller microcomputers (Digital KXT-11's). Each slave microcomputer can provide switching commutation pulses to control independently the pulse duration of power outputs from the 16 d.c. power supplies feeding the CI pulse transformers. Each slave controller also provides 16 switch commutation pulses to individual snubbing circuits which are used to control the voltage spikes which normally occur when inductive circuits are abruptly open-circuited. Thus each of the slave processors has the real-time capability of controlling all of the switching requirements for approximately 48 electrode pairs, or groups of electrodes if partial diagonal connection is assumed (at 60 Hz). If a more complex switching algorithm is required, such as any requirement to detect and react dynamically to variable electrode voltage output behavior, the capability would be significantly reduced. The Digital Microvax II master controller I/O bus has a capacity of 14 KXT-11 slave processors and is thus capable of expansion to a very large number of sources with no software programming modifications. Only one KXT-11 slave microcontroller is in the present system. computer control of the PASC process will permit synthesis of arbitrary shaped pulsed waveforms, the sinusoidal algorithm was initially chosen for study implementation because of its importance in nearly all applications and the fact that transformers were chosen as the consolidation device which restricted the generated outputs practically to waveforms having zero dc average content. Since the slave processors may be interrupted by the master controller, provision is made for a.c. parallel fault interruption and isolation from the multi-source dc system in a matter of microseconds. This eliminates the usual need for expensive dc switchgear.

The digital switching control codes for the KXT-11 slave processor have been written using the Micro-Pascal real-time software development toolkit purchased from Digital Equipment Corporation. All of the control software is thus written and debugged in Pascal on the Microvax II and is downloaded into KXT-11 single board computer (SBC), for subsequent execution. The input/output features of the KXT-11 SBC used to control the PASC system are the two bidirectional 8-bit input/output ports and the 4-bit control port. These three ports function with the control storage and buffer interface cir-

cuitry to generate the 32 switch point and snubbing GTO control pulses and also provide for 16 digital status point monitoring within the PASC system as shown in Figure 4.

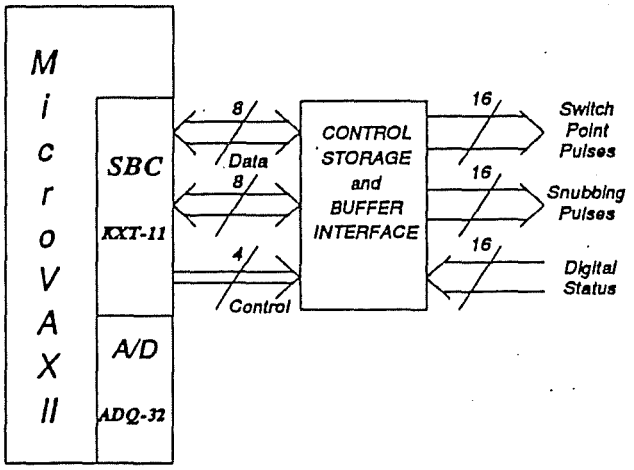

Figure 4 PASC CONTROL COMPUTER INTERFACE

Although a commercial implementation of the PASC technology would employ fiber optic GTO switching signals from the control computer to protect from elevated electrode voltages present along a MHD channel, the FDEF employs conventional wire cable switching signals with optical isolators to reduce cost. Thus each of the switch point and snubbing control pulse lines drive isolated GTO gate control circuits as shown in Figure 5.

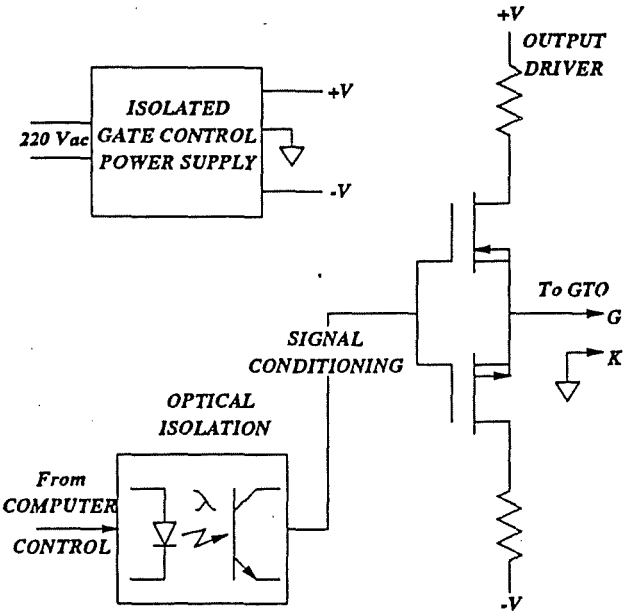

Figure 5 GTO GATE CONTROL CIRCUITS.

Isolation of these circuits is provided by the optical isolator connection of the control pulse lines (approximately 2.5 kilovolts) and the isolated dual output power supply for circuit operation. The output driver produces approximately 1 ampere sourcing and sinking current for the GTO gate-cathode circuit.

c. Design and Implementation of the Power Injection Circuitry

The power is injected into the PASC output consolidation and waveform synthesizing transformers (T-0 through T-7), by means of 16 autonomous dc power supplies. Each transformer has two primary windings as shown in Figure 6.

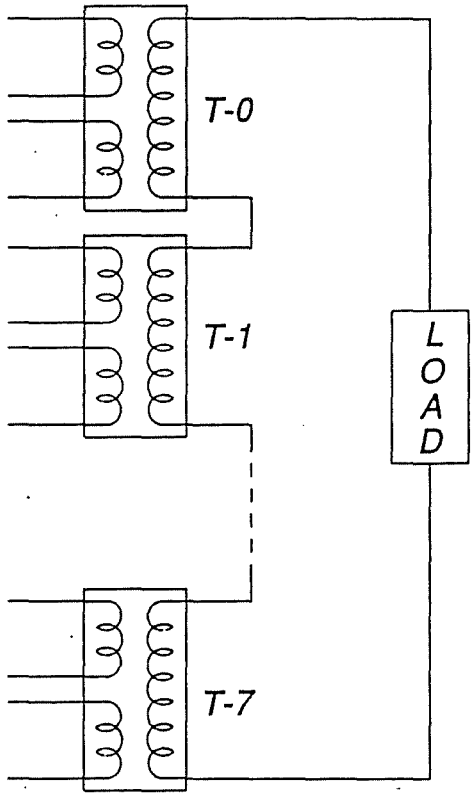

Figure 6 TWO PRIMARY WINDING CI TRANSFORMERS WITH SERIES CONNECTED SECONDARIES

The eight transformers used are standard 120/240 to 240/480 volt, 3 kilovolt-ampere, 60 hertz, single phase commercially available units. All primaries are independently switched and snubbed and are dc isolated from one another. The eight transformer secondaries are connected in series to drive the load bank. Figure 7 shows the transformer primary circuit connection. Each primary circuit has a 110 volt, 20 ampere power source, switch point GTO with gate control circuit, and snubbing GTO with gate control circuit.

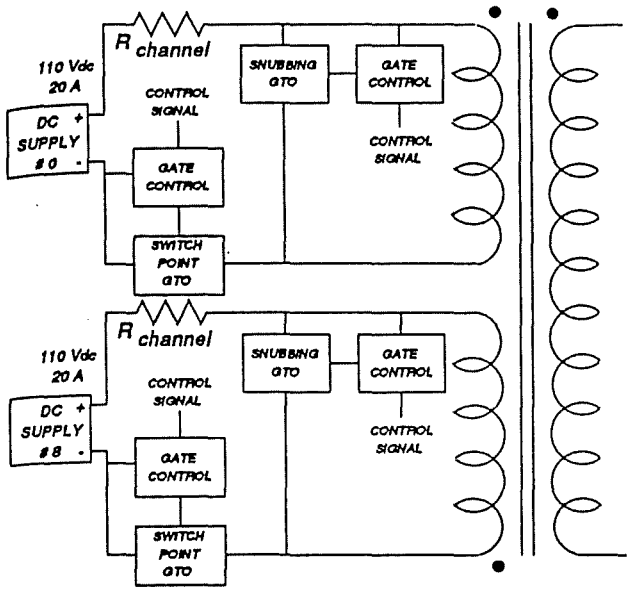

Figure 7 PRIMARY POWER INJECTION AND SNUBBING CIRCUIT

The switch point GTOs are 1000 volt symmetrical units with 80 ampere rating. The snubbing units are 1000 volt asymmetric units with 14 ampere rating. An antiparallel diode is used with these units to provide symmetric operation. The $R_{channel}$ resistors are used to simulate a static value of source impedance. Source resistor resistance values of 2.5, 5, and 10 ohms can be set by appropriate interwiring of two 5 ohm power resistors.

d. Measurement and Data Acquisition Design

The FDEF employs a data acquisition system consisting of a Tektronix sampling oscilloscope with direct on-line digital printer display for "snapshot" data presentation along with a conventional 16 channel multiplexed, 12 bit analog-to-digital converter controlled by the master control Microvax. The collected data, which can be taken at very high rates, is stored on Winchester disk for post-test plotting and analysis of results. For document presentation purposes, the "snapshot" results from the Tektronics oscilloscope are also input to an IBM PC/AT system disk.

The data acquisition code was developed using DEC VAXlab software toolkit to provide the necessary control program for the DEC A/D converter module (ADQ-32), which occupies a Q-bus I/O slot as indicated in Figure 4. The converter has 16 channels of 0-10 volt range with 12 bit resolution. Data transfer from the ADQ-32 to the host computer is under DMA control. Standard power industry transducers for voltage (0-120 volt rms), current (0-5 ampere rms), and power (0-500 watts) are used to generate the isolated inputs for the converter as shown in Figure 8. These units are used to monitor the ac input to the 16 rectifier bridges which make up the PASC unconsolidated dc supplies and the consolidated output to the load bank. Standard current transformers (CT) and potential transformers (PT) are used to feed these transducers where parameter reductions are required. The output voltage transducer has been modified to also provide an instantaneous voltage sample. Switch point voltage and current are sampled using resistive voltage dividers to reduce parameter values to the A/D input levels.

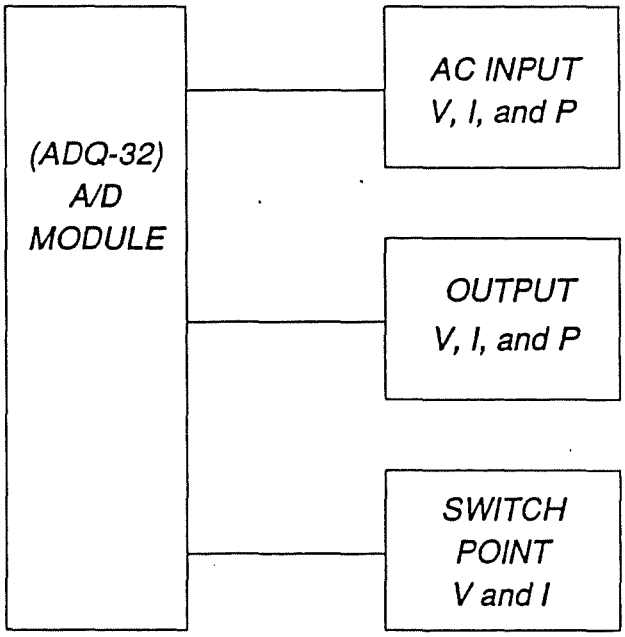

Figure 8 PROGRAM CONTROLLED DATA ACQUISITION

EXPERIMENTAL RESULTS

The FDEF implementation of the PASC technology has been used to study the production of sinusoidal signals of different frequencies, square and triangular output waveforms of different frequencies, and also the effects of various load impedances and different snubbing algorithms.

The FDEF has so far been used to study the feasibility of generating several types of waveforms digitally from 16 separate sources such as might represent a Faraday connected MHD generator. Both step-down and step-up transformer connections with series connected secondary windings have been tested to study the effects of loading-to-source impedance ratio effects on waveform distortion. Of the great amount of data collected, only a small sampling of the results are included in this paper. The experimental results shown below were obtained directly from the serial port of a digitizing oscilloscope and plotted using a standard commercially available plotting package.

Figures 9, 10, 11, and 12 depict the operation of the PASC system using a linear switching algorithm. In this mode of control, the SBC is programmed to initiate gate firing of the primary switch points at regularly spaced time intervals. This is the mode shown in Figure 3.

Figure 9 shows a case where the source resistance ($R_{channel}$ in Figure 7) is 10 ohms and the load is 100 ohms resistive. The CI transformers are in a 2:1 step down configuration and the 16 supplies are at 110 volts dc.

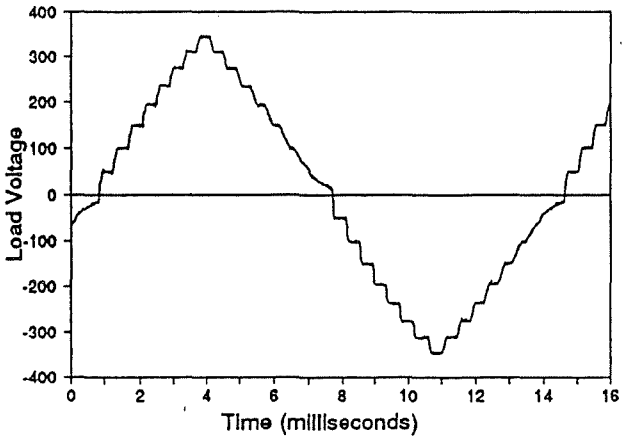

Figure 9 OSCILLOSCOPE OUTPUT INTO 100 OHM LOAD

Figure 10 shows a case identical to Figure 9 in all respects except the transformer configuration. In Figure 10, the transformers are in a 2:1 step up mode. The distortion from triangular in this case is cause by the current limitation imposed by the source resistance.

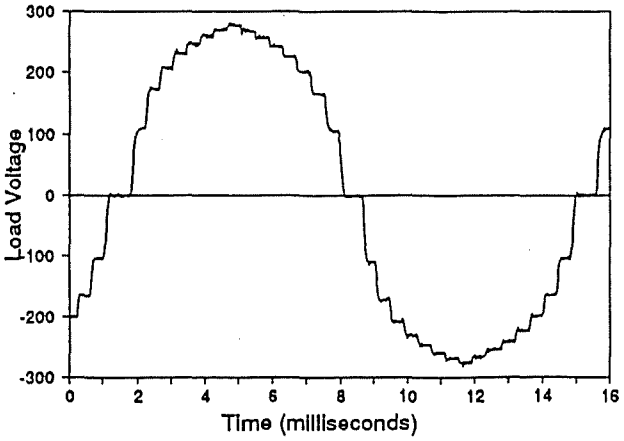

Figure 10 OSCILLOSCOPE OUTPUT INTO 100 OHM LOAD

In Figures 11 and 12, the load has been changed to 10 ohms resistive. Figure 11 shows a 10 ohm source with CI transformers in the 2:1 step down mode and in Figure 12 the mode of operation has been changed to step up.

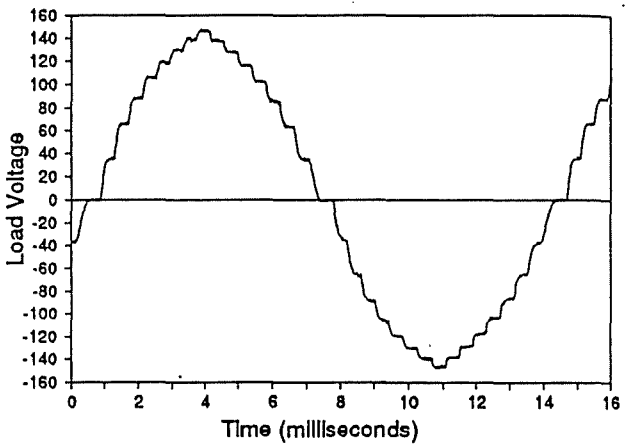

Figure 11 OSCILLOSCOPE OUTPUT INTO 10 OHM LOAD

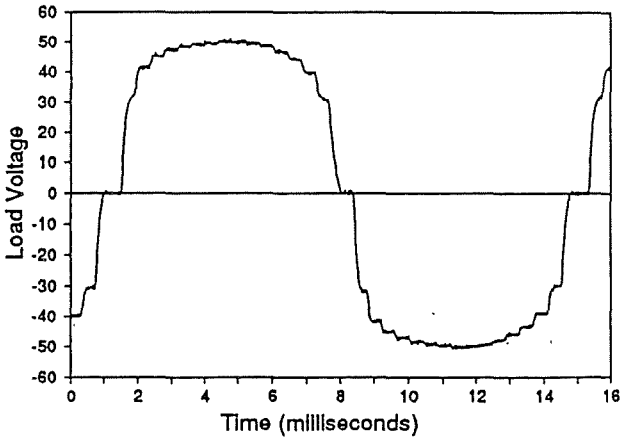

Figure 12 OSCILLOSCOPE OUTPUT INTO 10 OHM LOAD

With the heavier load imposed in these cases, the step up mode incurs a severe current limitation in the primaries and hence falls well short of the expected triangular output.

Again, SPICE and EMTP simulation results agree closely with these experimental results.

Figure 13, 14, and 15 are included to demonstrate the versatility of the PASC system consolidated output. Within the design window of the consolidation transformers, the ac output is limited only by the robustness of the controller as to waveshape and frequency. For these results, the dc supply voltage was reduced to 55 volts dc. Figure 13 shows a case in which the source impedance is 2.5 ohms, load is 100 ohms resistive, and the CI transformers are in the step up mode. Sinusoidal switching is employed to reduce harmonic content of the output waveform. The

term "sinusoidal switching" refers to the variable time delay between primary switch point firing programmed into the SBC in contrast to the constant time delay exhibited in Figure 3.

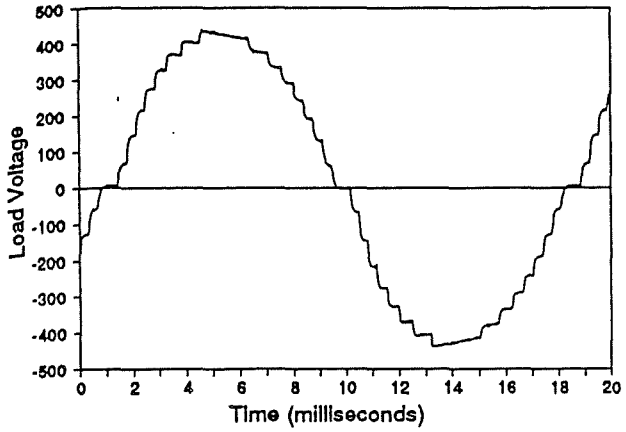

Figure 13 SINUSOIDAL OSCILLOSCOPE OUTPUT INTO 100 OHM LOAD

Figure 14 shows a square wave output in which several primary switch points are fired simultaneously. If consolidated, high voltage dc is to be the desired product, rectification of a square wave such as this may be a viable concept.

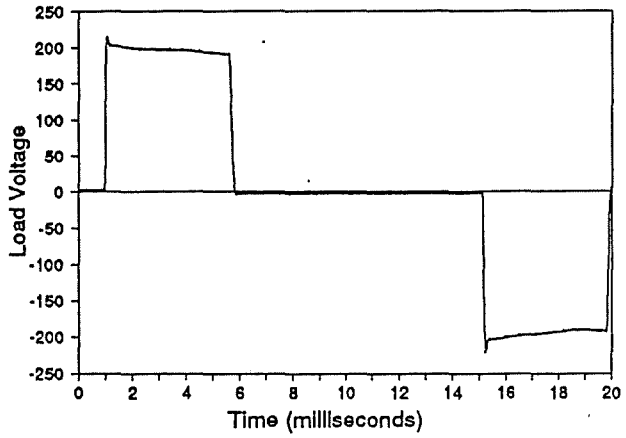

Figure 14 OSCILLOSCOPE OUTPUT OF SQUARE WAVE

Finally, Figure 15 shows a higher frequency output waveform. The filtering of the switched steps indicates that the upper limit of the window of operation of the CI transformers is being approached. The delay between positive and negative half-cycles is due to a time delay associated with an interrupt checking routine in the control algorithm and is in no way indicative of the performance of the system excluding the controller.

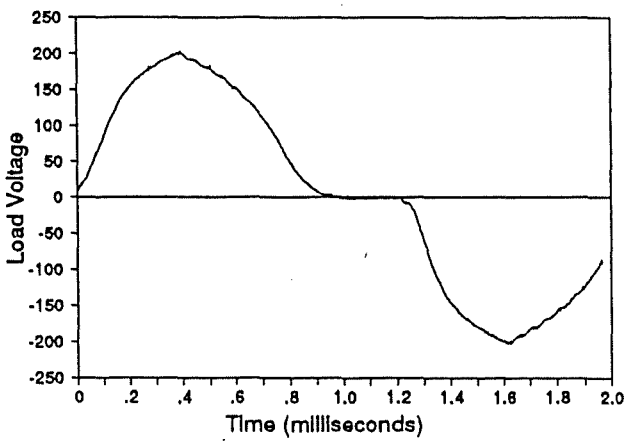

Figure 15 OSCILLOSCOPE OUTPUT OF 600 HERTZ WAVEFORM

PRELIMINARY SIMULATION RESULTS FOR THE DIAGONAL MHD CONFIGURATION

The diagonal MHD configuration is simulated by connecting the 16 primary circuits in parallel with one dc source and equivalent channel resistance. Figure 16 shows a case simulated on EMTP in which the source is 60 volts dc, the equivalent channel resistance is 1 ohm, and the load is 100 ohms resistive. Other simulation results show that the output is dominated by the ratio of source to load impedance.

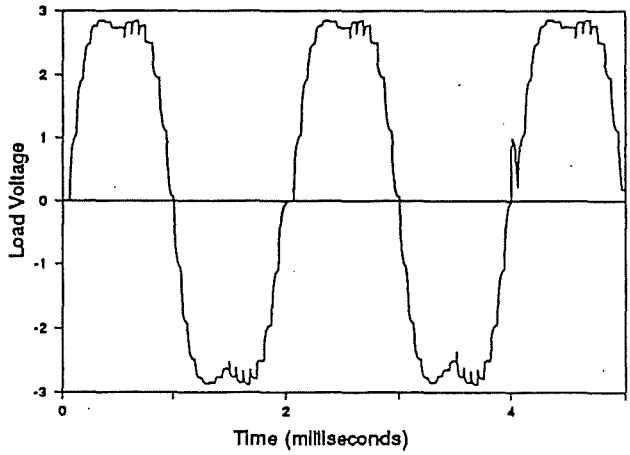

Figure 16 SIMULATION RESULTS FOR DIAGONAL CONFIGURATION INTO 100 OHM LOAD

CONCLUSIONS

The FDEF provides a cost effective way of studying the CI processes involved in extracting power from multiple sources of dc energy. Both distributed Faraday and diagonal type configurations can be studied by reconnection of the input connections for a wide variety of converter loading. As funds become available, future work will concentrate on the MHD diagonal connection and arrays of batteries, fuel cells, and solar cell.

ACKNOWLEGEMENT

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REFERENCES

[1]"Voltage Consolidation and Control Circuits for Multi-Electrode MHD Generators," R. S. Rosa, 15th SEAM, The University of Pennsylvania, Philidelphia, PA, May 24-26, 1976, p.VII.5

[2] "A Distributed Control System for MHD Generator Consolidation/Inverter System," R. Johnson, Journal of Microcomputer Applications, Vol. 1, No. 3, 1982.

[3] "Pulse-Amplitude-Synthesis-and-Control (PASC), of MHD Commercial Power Output," R. Johnson and V. Skurdal, 24th SEAM, Butte, MT, June 24-27, 1986.

[4] "A computer Controlled Electrode Consolidation/Force Commutated Thre Phase Inverter System for MHD Power Generation," K. Crissafulli, K. Marcotte, R. Johnson, and B. Jordan, 19th SEAM, UTSI, Tullahoma, TN, 1981.

[5] Dorrance L. Anderson, Albert E. Willis, and Carl E. Winkler, "Advanced Static Inverter Utilizing Digital Techniques and Harmonic Cancellation," NASA Technical Note D-602, NASA George C. Marshall Space Flight Center, Huntsville, AL, May 1962.